

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1           **Claim 1 (original):**   A wide band modulation PLL,  
2       comprising:  
3           a PLL part, including:  
4               a voltage controlled oscillator;  
5               a frequency divider that divides a frequency of  
6       an output signal of the voltage controlled oscillator;  
7               a phase comparator that outputs a signal based on  
8       a phase difference between a reference signal and the  
9       output signal of the frequency divider; and  
10           a loop filter that outputs an output to the  
11       voltage controlled oscillator so as to average the output  
12       of the phase comparator;  
13           a first modulation input part that inputs a first  
14       modulation signal to the voltage controlled oscillator  
15       based on inputted modulation data for modulating; and  
16           a second modulation input part that inputs a second  
17       modulation signal to a position different from the voltage  
18       controlled oscillator in the PLL part based on the  
19       modulation data,  
20           wherein the voltage controlled oscillator includes a  
21       first control terminal to which the first modulation signal  
22       is inputted and a second control terminal to which a signal

23       based on the second modulation signal is inputted; and  
24               wherein the first modulation input part has a  
25       modulation sensitivity calculation unit that calculates a  
26       first modulation sensitivity in the first control terminal  
27       and a modulation factor adjustment unit that adjusts a  
28       modulation factor of the modulation data based on the  
29       calculated first modulation sensitivity and outputs the  
30       first modulation signal.

1               **Claim 2 (original):** The wide band modulation PLL as  
2       set forth in claim 1, wherein the modulation sensitivity  
3       calculation unit has a modulation sensitivity calculation  
4       part that measures a signal inputted to the second control  
5       terminal, that calculates a second modulation sensitivity  
6       in the second control terminal, that measures a value  
7       indicating a ratio between the second modulation  
8       sensitivity and the first modulation sensitivity, and that  
9       calculates the first modulation sensitivity based on the  
10       calculated second modulation sensitivity.

1               **Claim 3 (currently amended):** The wide band modulation  
2       PLL as set forth in claim 1 ~~or 2~~, wherein the first  
3       modulation input part has an A/D converter that makes  
4       digital conversion of a signal inputted to the second  
5       control terminal of the voltage controlled oscillator, the  
6       modulation sensitivity calculation unit, the modulation

7 factor adjustment unit, and a D/A converter that makes  
8 analog conversion of an output of the modulation factor  
9 adjustment unit and that outputs the output to the first  
10 control terminal.

1 **Claim 4 (currently amended):** The wide band modulation  
2 PLL as set forth in ~~any one of claims 1 and 2~~claim 1,  
3 wherein the first modulation input part includes an A/D  
4 converter that makes digital conversion of a signal  
5 inputted to the second control terminal of the voltage  
6 controlled oscillator, the modulation sensitivity  
7 calculation unit, and the modulation factor adjustment  
8 unit;

9 wherein the modulation factor adjustment unit outputs  
10 a digital signal to the first control terminal; and

11 wherein the voltage controlled oscillator changes a  
12 frequency based on the digital signal inputted to the first  
13 control terminal.

1 **Claim 5 (currently amended):** The wide band modulation  
2 PLL as set forth in any ~~one of claims 1 through 4~~claim 1,  
3 wherein the second modulation input part has a frequency  
4 dividing ratio generation unit that controls a frequency  
5 dividing ratio of the frequency divider based on carrier  
6 frequency data and the modulation data.

1           **Claim 6 (currently amended):** The wide band modulation  
2       PLL as set forth in ~~any one of claims 1 through 4~~claim 1,  
3       wherein the second modulation input part has a direct  
4       digital synthesizer that generates a modulation signal  
5       based on carrier frequency data and the modulation data and  
6       that outputs the modulation signal to the phase comparator.

1           **Claim 7 (currently amended):** The wide band modulation  
2       PLL as set forth in ~~any one of claims 1 through 6~~claim 1,  
3       wherein the first modulation input part calculates the  
4       first modulation sensitivity, adjusts a modulation factor  
5       and outputs the first modulation signal at the time of an  
6       activation of the wide band modulation PLL and every  
7       predetermined period is elapsed after the activation.

1           **Claim 8 (original):** The wireless terminal apparatus  
2       incorporating the wide band modulation PLL according to any  
3       one of claims 1 through 7.

1           **Claim 9 (original):** A modulation factor adjustment  
2       method of a wide band modulation PLL comprising a PLL part  
3       including a voltage controlled oscillator, a frequency  
4       divider for dividing a frequency of an output signal of the  
5       voltage controlled oscillator, a phase comparator for  
6       outputting a signal according to a phase difference between  
7       a reference signal and an output signal of the frequency

divider, and a loop filter for averaging an output of the phase comparator and outputting the output to the voltage controlled oscillator, the method comprising:

inputting a first modulation signal to a first control terminal of the voltage controlled oscillator for modulating;

inputting a second modulation signal to a position different from the voltage controlled oscillator in the PLL part based on the PLL by inputting carrier frequency data;

calculating a first modulation sensitivity in the first control terminal of the voltage controlled oscillator, and

adjusting a modulation factor of the first modulation signal based on the calculated first modulation sensitivity.

**Claim 10 (original):** The modulation factor adjustment method of a wide band modulation PLL as set forth in claim 9, wherein the step of calculating the first modulation sensitivity comprises the steps of:

measuring an input voltage inputted to a second control terminal being different from the first control terminal in the voltage controlled oscillator based on the second modulation signal;

calculating a second modulation sensitivity in the second control terminal; and

11           measuring a value indicating a ratio between the  
12       second modulation sensitivity and the first modulation  
13       sensitivity, and calculating the first modulation  
14       sensitivity based on the calculated second modulation  
15       sensitivity.